TITLE OF INVENTION

INTERFACE DEVICE WITH STORED DATA ON TRANSMISSION LINES CHARACTERISTICS

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates to high speed communications, in particular, to an interface device between a transmitting device and a receiving device of a transmission system, wherein the transmitting device is capable of automatic compensation of cross-talk effects in the interface device by using information stored in an integrated circuit attached to that interface device. .

The present invention is particularly applicable to interfaces to logic and memory devices, to test equipment for testing semiconductor devices and to high speed communications.

Background of the Invention

It shall be appreciated that the invention can be applied to a wide variety of fields, though examples and background information, without limitation to the scope of the invention, represent automated semiconductor testing. Test equipment is typically used to determine whether a device under test ("DUT") follows a set of timing specifications. Accordingly, timing accuracy plays a vital role in the design of test equipment because a discrepancy in the timing accuracy can result in an incorrect classification of a DUT.

A typical test equipment comprises a tester and a device interface board (DIB) connected thereto. A test socket adapted to receive a DUT is mounted on the interface board. A plurality of transmission lines such as coaxial cables or strip lines are provided which join contacts of the test socket and junctions of the interface board with the testing device. The tester and the interface board are interconnected by urging pin electrodes provided on one of them against planar electrodes provided on the other, by pressing planar electrodes provided on both of them against each other, or by engaging connectors provided on both of them with each other. A device to be tested is mounted on the test socket.

A signal generator in the tester generates a test signal of logical levels at specified timings, based on a pattern and a timing signal. The test signal is converted by a driver in the tester into a signal voltage of a predetermined level such as the ECL or TTL level, which is supplied from the tester to pins of the DUT via the transmission lines of the interface board. Then, the resulting DUT output response signals are provided via the transmission lines to the tester, wherein they are compared by a comparator with a reference voltage for the decision of their logical level. Each logical signal based on the decision is compared by a logical comparator with an expected value pattern contained in the data pattern, and the output from the logical comparator is used to determine whether the DUT is good or bad.

In this instance, it is necessary that the timing for sending out the test signal and the timing for fetching the DUT output response signal in the tester be determined taking into account not only the relative delay times between respective circuits in the tester corresponding to the pins of the DUT or delays in the transmission lines but also crosstalk or crosstalk artifacts times of the transmission lines of the interface board which are connected to the pins of the DUT.

The following methods have been proposed to adjust the test signal send-out timing and the DUT output response signal acquisition timing.

According to one of these methods, the transmission lines are made equal in length to make the above-mentioned delay times in the interface board constant, and in the tester, the above-said timing is corrected using data on the constant time. This method suffers from differences between the physical length – all wires are normally the same actual length, and the electrical length for a given pattern. According to another method, the actual lengths of the transmission lines and the delay times are measured, the measured data are stored in a memory provided in the tester and the above-said timing is adjusted using the data read out of the memory. This method tries to adjust delay times by measuring the electrical length of isolated traces. In practice, the electrical length is influenced heavily by crosstalk, so the electrical length during measurement is not an accurate representation of the electrical length in service.

According to still another method, such as described in US 5,225,775, the DUT connection board is equipped with a nonvolatile storage for storing data on the delay times in the transmission line on the connection board corresponding to each terminal of the device under test, and the tester main body unit is so constructed as to adjust the test signal send-out timing and the device output response signal acquisition timing based on the data read out of the storage. Storing the actual topography and topography dependent parameters in a serial presence detect (SPD) memory and adjusting a control signal accordingly is known also from US 6,321,282. This suffers the same problems as previously mentioned, i.e. the electrical length during isolated test differs from that in service due to the neglect of the crosstalk coefficients.

According to US 5,225,775, a calibration procedure is performed by selecting one of a plurality of transmission lines on the connection board and measuring a time required for a signal to pass via this connection board, while all the other transmission lines are silent. Thus, cross-talk from adjacent lines is not taken into account.

As the speeds at which electronic devices operate have increased dramatically and it is not uncommon for these memory devices to run at frequencies at or greater than 100 MHz, the above mentioned methods fails to provide an adequate accuracy of timings. To test at such high frequencies, tester systems include a clock running at or above the maximum frequency at which devices can be tested. As clock frequencies increase, factors such as transmission line crosstalk or crosstalk artifacts such as uneven transmission line performance become significant. To compensate for such variations, some tester systems, such as production-oriented automatic test equipment (ATE) testers, use very high frequency (some as high as 1GHz) to provide very fine resolutions. However, in these systems crosstalk in signal paths can influence greatly the accuracy of calibration.

Still one more problem arises when the number of testing signals required to test a semiconductor device increases and it becomes more and more complicated technically to compensate timing errors for individual signals in each separate transmission line.

The similar problems arise in high speed communications where it is required to reduce artifacts introduced into a communication channel from the limited and non-

linear characteristics of the channel, such as by reflections not being absorbed efficiently or cross-talk between the transmission lines.

BRIEF SUMMARY OF THE INVENTION

Generally, the present invention is directed to an interface device, such as between a transmitter and a receiver in a communication channel, or such as an interface board for a tester system, provided with a means to compensate for uneven transmission line performance, e.g. caused by crosstalk or crosstalk artifacts using stored data on transmission characteristics.

According to one aspect of the invention, an interface device is provided for connecting a transmitting device having a first plurality of terminals and deriving a plurality of signals of a predetermined data pattern, the signals being arranged in groups, and a receiving device having a second plurality of terminals for receiving said signals;

the interface device having, respectively, input connectors connectable to said transmitter's terminals and output connectors connectable to said receiver's terminals, the inputs and outputs being interconnected by transmission lines within said interface device, the transmission lines being arranged in groups corresponding to said groups of signals; and

a storage for storing data on interconnections between said first plurality and second plurality of terminals and data on timing errors caused by crosstalk in each said group of transmission lines, measured with respect to a reference signal and relating to a specific data pattern, for each of said stored interconnection;

wherein the transmitting device is capable of compensating for timing errors in said groups of transmission lines using data read from said memory storage.

In another aspect, a test system is provided incorporating the interface device according to the invention.

In still another aspect, a method of compensation of timing errors in transmission lines is provided comprising the steps of:

- transmitting via transmission lines a plurality of signals of a predetermined data pattern to be applied to a semiconductor device, the signals being driven in groups;

- comparing the output response of a group of signals with a reference signal level;

- storing in a non-volatile memory data on timing errors in said transmission lines relating to specific data patterns, for each separate group of signals; and

- compensating for timing errors in said transmission lines for each said group of signals using said data read from said nonvolatile memory.

In still another aspect, a method of testing semiconductor devices employing the above method of compensation is provided.

In Fig.5, a typical interface device 52 according to the invention is shown having a plurality of transmission lines within the device (not shown), input connectors 57 for connecting to a tester head, a DUT socket 55 with output connectors 51 for connecting to a DUT and a storage 54 for storing data on interconnections and correction coefficients for compensating for timing errors caused by crosstalk in transmission lines.

According to the present invention, a tester interface such as a DUT interface board (DIB) is equipped with a means for storing the results of measurements of transmission line behavior caused by the combination of crosstalk or crosstalk artifacts and physical manufacturing tolerances or impedance errors in signal paths in a test head and interface board. The timing errors are measured for a group of signals and compensated by applying correction coefficients to a whole group of signals which provides increasing greatly the effectiveness of compensation and reduces time consuming calibration operations. In testers, the information is used to enable accurate calibration of timings of signals associated with a DUT.

In the testing equipment of the above construction according to the present invention, the length of the transmission lines on the interface board corresponding to the respective groups of terminals of the DUT are all known precisely from PCB design software. This software enables the DIB card to be designed so as to completely eliminate inaccuracy caused by errors in trace lengths. What remains are

manufacturing errors and crosstalk. While manufacturing errors may be measured at the production stage and the resulting correction coefficients may be stored in a memory storage mounted on a DIB, the effect of crosstalk is still the key source of inaccuracy left which depends on particular data pattern. Measurements of crosstalk and compensation thereof automatically equilibrates variations in manufacturing impedance due to fluctuations in PCB manufacturing process such as fluctuations in thickness, dielectric constants and other technology and material parameters which may be revealed to different extent during usage.

According to the present invention, the data on crosstalk and crosstalk artifacts is stored together with the information about interconnections required for a certain type of the DUT. The data on interconnections is stored in a storage device attached to the DIB and is retrieved automatically when the test is started. As the crosstalk and crosstalk artifacts depend on particular interconnection scheme, the measurements are conducted not only for each test pattern, but for each card interconnection. This is useful as the variety of DUT form factors requires many different DIB cards to be used in connection with each different DUT type. Though the interconnections for different DUT types are different, to unify the DIB card treatment by software, it is very convenient to store the information about DIB card interconnections comprising crosstalk information, in DIB card itself. A more detailed description of the DIB card of the present invention is presented in Attachment A.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Fig. 1 is a schematic block diagram of a testing device according to the invention;

Fig. 2 is a block diagram illustrating example equipment for measurement of crosstalk in transmission lines of a DIB according to the present invention;

Fig. 3 is a flowchart of the method of compensating crosstalk in test results;

Fig. 4a is a diagram explaining the influence of crosstalk in the transmission lines of the interface board;

Fig. 4b is a graph illustrating a calibration procedure in relation to reference signal, wherein the calibration is performed at a rising edge of a clock signal;

Fig. 4c is a graph illustrating a calibration procedure in relation to reference signal, wherein the calibration is performed at a falling edge of a clock signal;

Fig.5 is a plan view of an example embodiment of the device interface board.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will be further described in detail with reference to the accompanying drawings illustrating an example embodiment of the device interface board for an IC tester. However, it shall be appreciated that the present invention is not limited to ATE and may be equally employed by a specialist in the art to communication equipment.

As shown in Fig.1, the DUT testing device is provided with a tester 1 and a device interface board (DIB) 2. The tester includes a clock generator 11, a pattern generator 12, timing control circuits 13, drivers 14, receivers 15 and fault comparator 16 for storing the data for cycles containing differences between data provided by pattern generator 12 and DUT 3. Delays 4, 5, 6 are used to provide compensation for timing errors in transmission lines within interface device 2. The tester is controlled by a computer 18 through interface 17. The controlling computer may be external as well as an internal computer may be provided.

The clock generator 11 generates, based on an internal operation clock CLK, a clock signal to be applied to the drivers 14, receivers 15 and DUT 3 through timing control circuits 13. Timing control 13 comprises a means to control the crosstalk or crosstalk artifacts in output signals from drivers 14 and crosstalk or crosstalk artifacts in receivers' 15 clock signals. The pattern generator 12 operates in synchronization with the system clock CLK from the clock generator 11 to generate patterns to be provided via timing control 13 to the terminal pins of the DUT 3.

The DIB 2 comprises a storage 4, such as non-volatile memory, e.g. flash memory, for storing data on timing errors caused by crosstalk or crosstalk artifacts in transmission lines in the board 2 corresponding to each terminal of the DUT to make corrections to the results of tests based on the data read out from the storage 4. The storage memory shall be of a type allowing to read/write data after each calibration procedure and store them when the device is switched off.

The fault comparator 16 compares the obtained signal from the DUT with the expected value from the pattern generator 12 to produce test results which are downloaded by the computer 18 through interface 17 for further processing by a computer software. The said software uses the crosstalk or crosstalk artifacts data stored in the storage 4 for compensating timing errors in final results for a current data pattern. The same data may be used to manage the timing control circuitry 13 to compensate effects of crosstalk for each particular pattern by adding these data to values which shall define crosstalk or crosstalk artifacts in drivers 14.

The above test system may be essentially the same as disclosed, for example, in U.S. application Serial No.60/209,613 "Test systems for protocol memories" filed on 06 June 2000, or PCT/RU01/00234 filed on 06.06.2001, the specification of which applications is incorporated herein by reference.

As shown in Fig.2, on the interface device 22 which is in this example a device interface board (DIB) there is mounted the DUT socket 25 and the transmission lines 26 are provided within the DIB 22 which connect contacts of the socket 25 to the junctions between the DIB 22 and the tester 21.

The lengths of the transmission lines 26 are the same. Though the transmission lines are separated as a rule by insulation material, they have mutual capacitance and inductance caused by magnetic and electric fields having areas of intersections of force lines as illustrated in Fig.4. This cross-talk influence is exacerbated in synchronous systems wherein all the signals are synchronized, i.e. they change state at one and the same time. These effects cause a part of the signal to penetrate from one transmission line into another. As a result, a moment when the signal crosses the threshold at the output of transmission line depends on signals in other transmission lines, i.e. it depends on a particular data pattern. Thus, one of the important features of the present invention is that the timing errors caused by crosstalk effects are measured when the tester is running a test pattern to provide compensation of the timing error caused by this particular combination of signals. The knowledge of the influence of the signal crosstalk for each data pattern provides a basis for crosstalk compensation for each data pattern. Another important feature is that the timing errors are measured for a group of signals and the compensation

coefficients are applied to these groups also to adjust the position of this group in whole with respect to a reference signal.

To the contrary, according to a method as described in US 5,225,775, the measurements of the delay times and storing of the measured data into the storage are performed on the stage when the interface device has been fabricated, i.e. with no regard to a particular test pattern, also, the possibility of correcting these data during the exploitation of the interface device in a particular application is neither proposed, nor surmised.

Moreover, according to the known method, the delay times are stored for each transmission line and correction is applied to each signal. However, in practice, in high speed transmission of signals, it has been discovered that the skew between signals within one group is relatively low comparing to the skew between different groups of signals. Thus, it is assumed in the present invention that the timing skew of individual signals within one group is less than the skew of the group of signals in whole. For example, the group skew equal to $\pm$250 ps means that the individual signal skew is lower than $\pm$250 ps.

Fig. 2 illustrates a method according to which the aforementioned timing errors caused by crosstalk in the transmission lines of the interface device are measured and the measured data is stored in the storage on the interface device.

The interface device 22 comprises socket 25, which can be for example, a DIMM socket. During the calibration, no DUT is mounted on the interface device. Instead, preferably, a crosstalk card 27 is installed in DUT socket 25. Generally, the crosstalk card is a PCB having no electronic components mounted thereon and comprising contact points 28 which correspond to contact points of a real DUT (e.g. a DIMM) and which are made connectable to oscilloscope probes 29. To provide maximum accuracy of measurements, the crosstalk card preferably has transmission lines of minimum electrical length and the test points arranged closely to the ground point.

However, in a general case, the use of this card is not necessary, while the probes may be connected directly to interface device 22 close to the DUT socket, or another suitable device may be used for this purpose.

A tester, such as a conventional tester for testing synchronous memory, e.g. BT72 manufactured by Acuid Corporation Limited (Guernsey), comprising a tester head 21 and a tester main body (not shown in Fig.2), is powered on, and the selected data pattern is running. The tester shall be fully in operation and the tester head's flash memory (SPD, serial presence detect) and an interface device 22 shall be initialized with start-up values. At this stage the SPD Reader/Writer software tool is used to initialize the tester head's SPD. The next step is initialization of an SPD installed on the interface device 22.

The SPD installed on the interface device, or DIB (device interface board), is generally designed so that it comprises at least three arrays of data that is read by the tester and provided to the controlling computer. In the first array, the number and type of the connector of the DIB is stored. In the second array, a table is stored relating to interconnection of contacts of the DUT and test signals. In the third array, correction coefficients are stored that are written to this memory during production and bears information on timing errors in transmission lines, measured during calibration. These correction coefficients are further adjusted according to the invention for crosstalk timing errors.

To obtain the required accuracy of measurements, an oscilloscope 20 is used, which may be a calibrated 1GHz bandwidth, 4GS/s sample, or better version digital oscilloscope having at least two active probes having input capacitance not more than 1 pF, for example, TDS794 manufactured by Tektronix Inc. (OR). One probe of the oscilloscope is connected to the crosstalk card 27 at a point CK_0 providing a signal used for triggering the scope, preferably, a clock signal. The second probe of the oscilloscope is connected sequentially to each of the other signal lines.

The signals are grouped in accordance with its functionality, so that, for example, data signals are arranged in separate groups, clock signals are arranged in other separate group, DQ (bi-directional data) signals are arranged in another groups. An example of typical signal grouping is shown in Appendix B.

The crosstalk timing error of a selected group of signals is measured with respect to the reference clock signal CK0. Another clock signal CK1 is used to trigger the scope. Note that, for timing error measurement, all signals are observed on test

points of crosstalk card 27. Both rising and falling edges of a signal being measured are to be considered. To observe them simultaneously, the scope shall be configured so as to accumulate waveforms with reasonable persistence and triggered from a clock signal.

Timing error measurements are performed whilst the system is running a special crosstalk test. This test is running continuously to generate transitions on all signals to be checked. To achieve the best possible precision and resolution, the scope should have only one channel activated when taking measurements. This will ensure that the total sample rate is not divided between several channels but fully assigned to the channel which is used for measurements. The other channel is only used to trigger the scope. For a DDR memory, differential signals are used for measurements.

Before skew measurements, a clock signal delay is measured to provide high accuracy in subsequent calculations.

For initial tuning, a trigger channel connected to CK1 is enabled and trigger level is adjusted, for example, to 1.4 for SDR memory, or 1.25V for a DDR type memory. When the expected rising edge of the clock is observed, the other channel is connected to CK0. This channel is selected as a reference signal for crosstalk measurements. A rising edge of the signal CK0 is selected close to the edge of CK1, and then, the first channel (CK1) is disabled.

If the timing error is measured at 1.4V level, the vertical position of the displayed signal shall be adjusted accordingly, so that the scope's central horizontal line would correspond to the 1.4V level. To measure time intervals, vertical cursors are enabled. The first cursor is set to the point where the center of the clock edge crosses the 1.4V level. Then, the second cursor is selected for measurements, while the position of the first one remains constant, as illustrated in Fig.4b and Fig.4c, where example diagrams are shown for SDR memory. It shall be mentioned that one and the same scope channel is used for both the reference and measured signals.

The measuring probe is disconnected from CK0 and connected to a signal that is chosen for timing error measurement. Using the second vertical cursor, two crosstalk measurements are made on each signal, to define the leftmost (T_{left}) and

rightmost (T_{right}) timing error caused by crosstalk in transmission line. The leftmost timing error is measured at the leftmost point where signal traces cross the selected level on the scope's screen. The rightmost timing error is measured at the rightmost point where signal traces cross 1.4V level on the scope's screen.

The individual signal timing error is a signed value. For points on the left of the reference cursor (read: of the Clock edge) the timing error has a negative value. For points on the right of the first cursor the timing error has a positive value.

The procedure of crosstalk adjustment is iterative, and several iterations of full measurement may be preferably needed.

According to the embodiment of the invention where all fast output signals on the header are driven by multi-bit registers, and each register has its own delay vernier, such as described in PCT/RU99/00194 filed on 10.06.1999, the signals are grouped so that the signals controlled by a selected vernier form one group, and signals controlled by different verniers, form different groups. The skew measurements are performed for groups of signals instead of performing measurements for each individual signal, thereby, the accuracy of measurements is increased and the time consuming measurement operations are reduced.

According to another embodiment, signals are grouped with respect to pin cards, so that the signals relating to a selected pin card form one group. Other criteria may be chosen to group the signals and obtain the advantages mentioned above.

At the first stage, the crosstalk timing error is adjusted in each group of signals. In a first iteration, in each group only a signal having leftmost timing error and a signal having rightmost timing error are considered. The average of these two values is calculated as T_{update}, as shown below.

The update T_{update} to the propagation time for a given group is an additional delay value required to make the leftmost and the rightmost timing error symmetrical with respect to the reference clock. The update value is calculated as follows:

$$T_{update} = (T_{left} + T_{right})/2,$$

where

T_{left} is a minimum left crosstalk timing error value among all the individual signal timing errors measured for signals of the given group;

T_{right} is a maximum right crosstalk timing error value among all the individual signal timing errors measured for all signals of the given group.

The T_{update} is passed on to the SPD card and used further by vernier to shift this group of signals so that the group is centered at this average value at the next step of iterations. Preferably, when the leftmost and the rightmost deviation from the reference are counted in each group, further iterations are performed using only these measurements, and T_{update} values for groups are calculated for all iterations except the final one. The final measurement must be complete to ensure the maximum timing error requirement is met on all signals.

To facilitate the calibration, a special update table may be used with pre-calculated results. The table contains minimum and maximum timing error values entered during current iteration to the table for each group. Update values are calculated for each group in the bottom row of the table and shall be entered in to the respective group tables. As the update values are used in further calculations, they can be adjusted directly in the respective cells of the group tables.

The method of the invention is further illustrated with reference to Fig.3.

First, the memory storage that is mounted on the DIB, is initialized, i.e. some initial values shall be written in the memory, for example, zero update values. Second, the calibration procedure is running. The signal crosstalk artifact, such as delay, is measured as has been described in details above. Next step is measuring timing error with respect to the reference clock for fast DUT signals which are most likely to produce minimum and maximum timing error.

An example table providing typical DUT signals, which produce minimum and maximum skew in each Delay Vernier Group is shown below. This example is valid for SYNBASED baseboards and HDRDIMMG header boards.

Delay Vernier Group	Minimum Skew	Maximum Skew
7	DQ10, DQ36	DQ8, DQ38
8	DQ37	DQ39
11	DQ48	DQ60
12	DQ49	DQ63
10	BA1	A4
9	CB0	CB6

13	DQMB1	DQMB7
14	WE	CKE1
15	S2	S0

Once the reference line is selected and the position of the reference signal is fixed on the scope, a crosstalk timing error is calculated as defined by time difference between the position of the measured signal and the position of the reference signal, to obtain thus the relative values in respect to the selected reference. If the crosstalk timing error for these signals is within the desired range, e.g. within ±250ps for the DDR memory, then, measurements are considered to be completed and the values are stored, otherwise, compensation coefficients are updated and the iterative procedure is continued as has been explained above.

The obtained relative data at the end of the measuring procedure is stored in the flash memory 4 for further usage by the controlling computer software as described above in detail.

As shown in a flow chart in Fig.3, the above procedure, as has been mentioned already, has an iterative character because the resulting crosstalk artifacts changes each time when a new compensation values applied and is performed sequentially until the crosstalk timing errors are minimized for a predetermined range when a single time control element, e.g. a vernier, is used to control several signals, or, eliminated, if each signal has a separate time control element.

The flow chart in Fig.3 can be further modified by adding a step of reading interconnection data or in other way within the scope of the invention as shall be evident for a specialist in the art.

Another example embodiment of the procedure of the invention with respect to DDR memory is illustrated in the Attachment B.

It shall be appreciated also that other embodiments and modifications of the present invention are possible within the scope of the present invention. Thus, the invention may be applied to compensating timing errors in communication systems that can serve to increase the bandwidth of signal transmission. It can be applied to reduce timing dispersion of a signal in cases when signals are transmitted via an optical cable and in various other applications.